REMARKS

This application has been carefully reviewed in light of the Office Action mailed on April 5, 2002. Claims 39-44 are pending in this application. Claims 39 and 42 have been amended. Reconsideration of the above-referenced application in light of the amendments and following remarks is requested.

Claims 39-44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable by Nakashima et al. (U.S. Patent No. 5,717,252) ("Nakashima") in view of Maruyama et al. (U.S. Patent No. 6,266,242) ("Maruyama") and in further view of Ishikawa et al. (U.S. Patent No. 6,158,116) ("Ishikawa"). Reconsideration is respectfully requested.

The present invention is directed at a processor system utilizing a ball grid array (BGA) semiconductor package having a low profile. Claims 39 and 42 have been amended to reflect this important feature.

Amended claim 39 recites a processor system comprising "a central processing unit . . . a memory device [comprising] . . . a plurality of low profile ball grid array semiconductor packages [comprising] a base substrate having a top surface and a bottom surface, with an aperture therein which extends from said top surface to said bottom surface, a series of conductive traces located on said bottom surface of said base substrate, a plurality of conductive balls connected to said series of conductive traces, a thin sheet material secured to said base substrate and covering said aperture such that a cavity is formed, said thin sheet material having a thickness of from approximately 0.025 to approximately 0.1 mm, and a semiconductor element mounted in said cavity."

Amended claim 42 recites a processor system comprising "a central processing unit . . . a memory device [comprising] . . . a plurality of low profile ball grid array semiconductor packages [comprising] a base substrate having a top surface and a bottom surface, said base substrate having an aperture extending from said top surface to said bottom surface, a series of conductive traces located on said bottom surface of said base

substrate, a plurality of conductive balls connected to said series of conductive traces, a thin sheet material secured to said top surface of said base substrate and covering said aperture to form a downward facing cavity, said thin sheet material having a thickness of from approximately 0.025 to approximately 0.1 mm, and a semiconductor element mounted in said downward facing cavity."

The subject matter of amended claims 39 and 42 would not have been obvious over Nakashima in view of Murayama. Nakashima provides a semiconductor device "which is highly reliable and easy to mount even when the bonding pad pitch is reduced" (Col. 1, lines 63-65). Nakashima teaches a device with a substrate (4) that surrounds a semiconductor chip (3). The recessed portion in Nakashima comprises a complex intermittent pattern of four layers of material, e.g., a structure of overlapping multiple segment layers. These materials comprise an insulating tape (2), conductor pattern (1), and two other layers formed on the conductor pattern (1) (Figs. 2(a) – 2(c), Col. 8, lines 26-57). The recessed portion is Nakashima is created by pressing a support base against the insulating tape (2). Furthermore, Nakashima teaches forming a recessed portion "by depressing the metal substrate 4 upward . . . [so that] it is almost level with the conductor pattern 1" (Col. 16, lines 5-12).

Murayama simply teaches an apparatus "which provides excellent heat release" (Col. 1, lines 47-48). Murayama provides a "processor . . . with [a] heat release plate in the bare-chip state, so that the heat radiated by the processor is conducted to the heat release plate from which the heat is dissipated" (Col. 1, lines 61-64). Further, "[t]he BGA used . . . has a gap of about .5 mm, which offers a sufficient thermal insulating effect." (Col. 4, 57-59). Murayama also teaches a bare chip "is a chip that has *no package made of resin*, for example and whose *metal is thus literally exposed*" (Col. 4, 9-11) (emphasis added).

The subject matter of amended claims 39 and 42 would not have been obvious over Nakashima in view of Murayama. Murayama is not directed toward forming a "low

profile ball grid array" as recited by amended claims 39 and 42. Further, Murayama teaches a BGA with a gap of about .5 mm. This is not a low profile BGA.

One skilled in the art would not have been motivated to combine Maruyama, which discloses an apparatus with a heat-releasing plate with a bare chip that has no package made of resin whose metal is exposed, with Nakashima, which discloses a structure of overlapping multiple segment layers with a chip surrounded by polyimide resin film. There is nothing in either references which suggest that its teachings would be applicable to the other. Each reference is directed to solving a different problem

Moreover, the subject matter of amended claims 39 and 42 would not have been obvious over Nakashima in view of Murayama, and in further view of Ishikawa. Ishikawa discloses a metal film 10 formed over the "principal surface of the insulating substrate 30; and a metal film 20 formed on the back surface facing the principal surface." Ishikawa teaches that "in order to attain sufficient radiation effects, the thickness of the metal film 20 is preferably about 100 um or more," and in order to provide external connections, the "thickness . . . is preferably 1000 um or less." (Col. 7, lines 42-47).

The Office Action contends, Ishikawa teaches a thickness for a metal film (20) in the range of 0.1 to 1.0 mm, which encompasses the range claimed in the present invention of "approximately 0.025 to approximately 0.1 mm" as recited by amended claims 39 and 42.

Ishikawa does not teach that the thickness of the metal film layer (20) can be between 0.1 and 1.0 mm. Ishikawa teaches that the outmost boundaries for the thickness of metal film (20) should be 0.1 mm or more due to radiation effects, and 1.0 mm or less due to external connections. Further, Ishikawa specifically teaches that "the thickness of the metal film (20) is in an approximate range from about 200 um to about 300 um, both inclusive." (Col. 7, lines 48-50). Thus, Ishikawa merely teaches that the thickness of the metal film (20) should fall between 0.2 and 0.3 mm. This is outside the ranges as claimed in amended claims 39 and 42. In addition, Ishikawa does not teach that the conductive

traces are connected to conductive balls. Accordingly, Ishikawa does not teach or suggest any modification of either Nakashima or Murayama which would attain the claimed invention.

Moreover, one skilled in the art would not have been motivated to combine Ishikawa, which discloses a metal film of 0.2 to 0.3 mm thickness, with Murayama, which discloses an apparatus with a heat-releasing plate with a bare chip that has no package made of resin whose metal is exposed, further with Nakashima, which discloses a structure of overlapping multiple segment layers with a chip surrounded by polyimide resin film. There is nothing in any of these references which suggest that its teachings would be applicable to the other two references.

Each reference is directed to solving a different problem. Ishikawa is directed toward "providing a radio frequency module . . . which can reduce the number if required components and . . . required process steps" (Col. 4, lines 41-45). Murayama is directed toward providing a processor with "pasted with [a] heat release plate in the bare-chip state, so that the heat radiated by the processor is conducted to the heat release plate from which the heat is dissipated" (Col. 1, 61-65). Nakashima is directed toward providing a device "easy to mount even when the bonding pad pitch is reduced" (Col. 1, lines 62-64). Accordingly, Murayama's, Nakashima's, and Ishikawa's inventions are not directed toward achieving a low profile semiconductor device.

Still further, even assuming arguendo that the references could be combined, at best, Ishikawa with Murayama with Nakashima, would only suggest a structure having a CPU module with a heat release plate in the bare-chip state with multiple-segment layered chip having a metal film 0.2 to 0.3 thickness. As described above, one specific goal of the present invention is to provide a low profile BGA, e.g., one having minimum overall thickness.

The combinations would not teach or suggest a computer system comprising, "a central processing unit . . . a memory device [comprising] . . . a plurality of low profile ball

grid array semiconductor packages [comprising] a base substrate having a top surface and a bottom surface, with an aperture therein which extends from said top surface to said bottom surface, a series of conductive traces located on said bottom surface of said base substrate, a plurality of conductive balls connected to said series of conductive traces, a thin sheet material secured to said base substrate and covering said aperture such that a cavity is formed, said thin sheet material having a thickness of from approximately 0.025 to approximately 0.1 mm, and a semiconductor element mounted in said cavity," as recited by amended claim 39 (emphasis added).

Further, the combinations would not teach or suggest a computer system comprising, "a central processing unit . . . a memory device [comprising] . . . a plurality of low profile ball grid array semiconductor packages [comprising] a base substrate having a top surface and a bottom surface, said base substrate having an aperture extending from said top surface to said bottom surface, a series of conductive traces located on said bottom surface of said base substrate, a plurality of conductive balls connected to said series of conductive traces, a thin sheet material secured to said top surface of said base substrate and covering said aperture to form a downward facing cavity, said thin sheet material having a thickness of from approximately 0.025 to approximately 0.1 mm, and a semiconductor element mounted in said downward facing cavity," as recited by amended claim 42.

Claims 40-41 depend from claim 39, and claims 43-44 depend from claim 42, and incorporate all of the limitations of claim 39 and 42 respectively, and for similar reasons described above, are not taught or suggested by Nakashima in view of Maruyama, and in further view of Ishikawa. Accordingly, withdrawal of the rejection of dependent claims 40-41, along with independent claim 39, and dependent claims 43-44, along with independent claim 42 is respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned, "**APPENDIX A**".

In summary, for all of the reasons set forth above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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APPENDIX A

39. (amended) A processor system comprising:

a central processing unit; and

a memory device connected to said central processing unit, said memory device comprised of a plurality of low profile ball grid array semiconductor packages, said low profile ball grid array semiconductor packages comprised of [an insulating] a base substrate having a top surface and a bottom surface, [said insulating substrate having] with an aperture therein [extending] which extends from said top surface to said bottom surface,

a series of conductive traces located on said bottom surface of said base substrate,

a plurality of conductive balls connected to said series of conductive traces,

a thin sheet material [approximately 0.025 to 0.1 mm thick] secured to said [top side of said] base substrate [to form a cavity] and covering said aperture such that a cavity is formed, said thin sheet material having a thickness of from approximately 0.025 to approximately 0.1 mm, and a semiconductor [die] element mounted in said cavity.

42. (amended) A processor system comprising:

a central processing unit; and

a memory device connected to said central processing unit, said memory device comprised of a plurality of low profile ball grid array semiconductor packages, said low profile ball grid array semiconductor packages comprised of [an insulating] a base substrate having a top surface and a bottom surface, said [insulating] base substrate having an aperture [therein] extending from said top surface to said bottom surface,

a series of conductive traces located on said bottom surface of said base

substrate,

a plurality of conductive balls connected to said series of conductive traces,

a thin sheet material [approximately 0.025 to 0.1 mm thick] secured to said [bottom side] top surface of said base substrate and covering said aperture to form a downward facing cavity, said thin sheet material having a thickness of from approximately 0.025 to approximately 0.1 mm, and a semiconductor [die] element mounted in said downward facing cavity.